REMARKS

Claims 1-4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hodate et al. (U.S. 5,518,940), taken with Yudasaka et al. (U.S. 5,563,427). Applicant respectfully traverses this rejection because neither of the cited references, whether taken alone or in combination, discloses or suggests offset regions, or that hydrogen ions cannot be implanted in the channel region under the gate electrode, as in claim 1 of the present invention, as amended.

Applicant maintains and incorporates by reference herein those arguments previously advanced on pages 3 through 6 of Amendment A, filed on July 2, 2001. Applicant respectfully requests that the Examiner reconsider those arguments, and withdraw this Section 103 rejection. Additionally, Applicant respectfully requests that the Examiner consider the following new arguments and expansions upon the previous arguments.

Claim 1 has been amended to positively recite offset regions, which regions are disposed between the lightly doped drain ("LDD") regions and the channel region. Such offset regions do not contain significant concentrations of impurity dopant, and are also effective for reducing the electric field. Neither Hodate nor Yudasaka discloses or suggests anything like the offset regions of the present invention. For at least these reasons, the rejection of claim 1 of the present invention based on a combination of Hodate and Yudasaka is respectfully traversed.

Moreover, neither of the two cited references teaches or suggests that hydrogen is excluded from the channel region. Hodate neither discloses nor suggests that hydrogen ions are implanted in any region of the thin film. The Examiner has, in Paper No. 12, cited only Yudasaka as standing for the implantation of hydrogen. However, Yudasaka suggests that hydrogen actually is implanted into the channel region.

As previously discussed in Amendment A, Yudasaka shows hydrogen implanted into the entire semiconductor film, including gate electrode 609 over the channel region 607. Although Yudasaka does not expressly state that hydrogen is implanted into the channel region, Yudasaka implicitly teaches that such would occur. Yudasaka expressly discloses that hydrogen is implanted at 80 keV (see col. 22, lines 53-55) or less, (see col. 21, lines 57-58), for a gate electrode thickness of 600 nm. (See col. 22, lines 47-48). Comparing these figures to Table 10 on page 10 of the Specification to the present Application, it can be seen that the hydrogen flight depth would be greater than the gate electrode thickness at the disclosed level of acceleration energy in Yudasaka. In other words, Yudasaka's gate electrode would not prevent hydrogen from being implanted into the channel region, which therefore teaches away from the present invention. Accordingly, for at least these additional reasons, the Section 103 rejection is respectfully traversed.

The present invention is designed so that hydrogen ions cannot be implanted into the channel region. This feature of the present invention provides advantages not realized by either of cited references. LDD regions are generally provided for reducing the

electric field -- particularly between the gate electrode and the heavily doped drain region. However, the level of electric field reduction realized by the LDD region -- as in the prior art -- is typically insufficient. Leakage current in the cut-off state is often still too large. The present invention addresses and solves this problem.

In the present invention, ion implantation is performed under such conditions such that impurity ions cannot be implanted through the gate insulating film, and hydrogen ions cannot be implanted into the channel region. This method thus enables light doping under low acceleration energy for the LDD region, as well as the production of an offset region between the gate electrode and the LDD region. This highly resistive offset region serves to further reduce the electric field around the drain junction, thereby further reducing the leakage current deterioration of characteristics by hot carriers. The prevention of hydrogen in the channel region further improves the reliability of the device formed by this method.

Neither Hodate nor Yudasaka addresses this problem faced and solved by the present inventor. The problem faced and solved by the present inventor is to be considered in determining the obviousness of combining references. Because neither of the two cited references addresses such a problem, the rejection for obviousness is improper. The Section 103 rejection is accordingly further traversed.

Claims 2-4 all depend either directly or indirectly from independent claim 1, and therefore include all of the features of the base claim, plus additional features.

Accordingly, for at least the reasons discussed above in traversing the rejection of claim 1, the rejection of claims 2-4 based on a combination of Hodate and Yudasaka is also respectfully traversed.

Claims 5-6 and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hodate with Yudasaka, and further in view of Yamazaki et al. (U.S. 5,523,257). With respect to claims 5 and 6, Applicant respectfully traverses this rejection for at least the reasons cited above in traversing the rejection of independent claim 1. Claims 5 and 6 both depend either directly or indirectly from claim 1. With respect to independent claim 22, claim 22 recites offset regions similar to those discussed above in traversing the rejection of independent claim 1, and is thus similarly distinguishable over the prior art of record.

As discussed previously and above, Hodate and Yudasaka both fail to teach or suggest offset regions or hydrogen exclusion in the channel region. Yamazaki merely discloses the use of laser annealing for re-crystallization and activation. However, Yamazaki neither discloses nor suggests offset regions, hydrogen implantation, or the exclusion of hydrogen from the channel region. Accordingly, the rejection of claims 5-6 and 22 based on a combination of Hodate, Yudasaka, and Yamazaki is respectfully traversed.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned "**Version with markings to show changes made.**"

For the foregoing reasons, Applicant submits that this Application, including claims 1-6 and 22, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1 and 22 have been amended as follows:

1. (Twice Amended) A method of manufacturing thin film transistors comprising the steps of:

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(i) forming a gate insulating film on each of the semiconductor layers;

(ii) forming a gate electrode on the gate insulating film over each of said semiconductor layers;

(b) implanting dopant into first regions at outsides of [a region] regions designated for offset regions adjacent to a channel region under said gate electrode in each of said semiconductor layers directly or through a thin insulation film whose thickness is equal to or less than 50nm by ion implantation to form lightly doped regions; and

(c) implanting dopant into outer regions within said first regions in each of said semiconductor layers directly or through said thin insulation film to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions[;].

wherein said ion implanting steps (b) and (c) are so selected that hydrogen ions are also implanted into said lightly doped regions and said heavily doped source/drain regions, but not into said channel region under said gate electrode[.], and

wherein said dopant cannot substantially be implanted into said offset regions.

22. (Amended) A method of manufacturing thin film transistors comprising the steps of:

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(i) forming a gate insulating film on said substrate, said film covering said semiconductor layers;

(ii) forming a gate electrode layer on said gate insulating film;

(b) implanting dopant into first regions at outsides of [a region] regions designated for offset regions adjacent to a channel region in each of said semiconductor layers directly or through a thin insulation film whose thickness is equal to or less than 50nm by ion implantation to form lightly doped regions;

(c) implanting dopant into outer regions within said first regions in each of said semiconductor layers directly or through said thin insulation film to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions; and

(d) irradiating a laser beam directly or through said thin insulation film to said first regions to activate dopants implanted in steps (b) and (c)[.],

wherein said dopant cannot substantially be implanted into said offset regions.